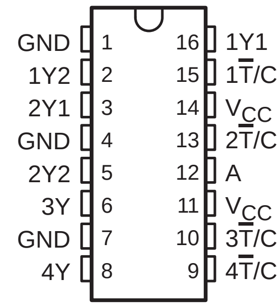
- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages**

D OR DB PACKAGE
(TOP VIEW)



description

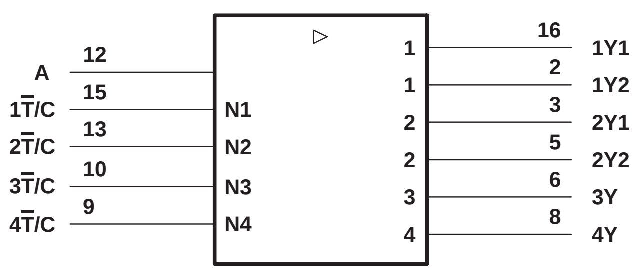
The CDC328A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ($\overline{\text{T}}$/C), various combinations of true and complementary outputs can be obtained.

The CDC328A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

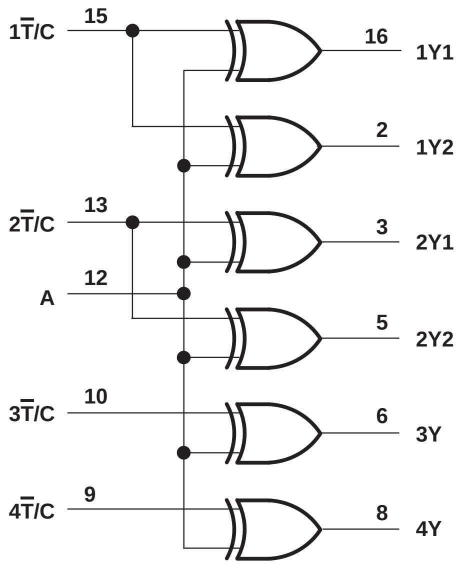
INPUTS		OUTPUT
$\overline{\text{T}}$/C	A	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package	0.77 W
DB package	0.6 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			–48	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

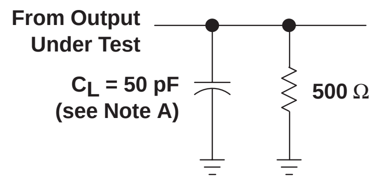
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 48 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA				0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	µA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–15		–100	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			10	mA
			Outputs low			40	
C_i	V_I = 2.5 V or 0.5 V				3		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

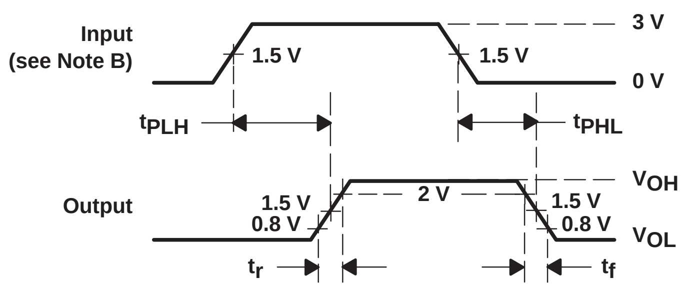
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Any Y	1.7	5	ns
t_{PHL}			1.5	5	
t_{PLH}	$\overline{T}$/C	Any Y	1.5	5	ns
t_{PHL}			1.4	5	
$t_{sk(o)}$	A	Any Y (same phase)		0.5	ns
		Any Y (any phase)		1	
$t_{sk(p)}$	A	Any Y		1	ns
t_r		Any Y		1.5	ns
t_f		Any Y		1.5	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

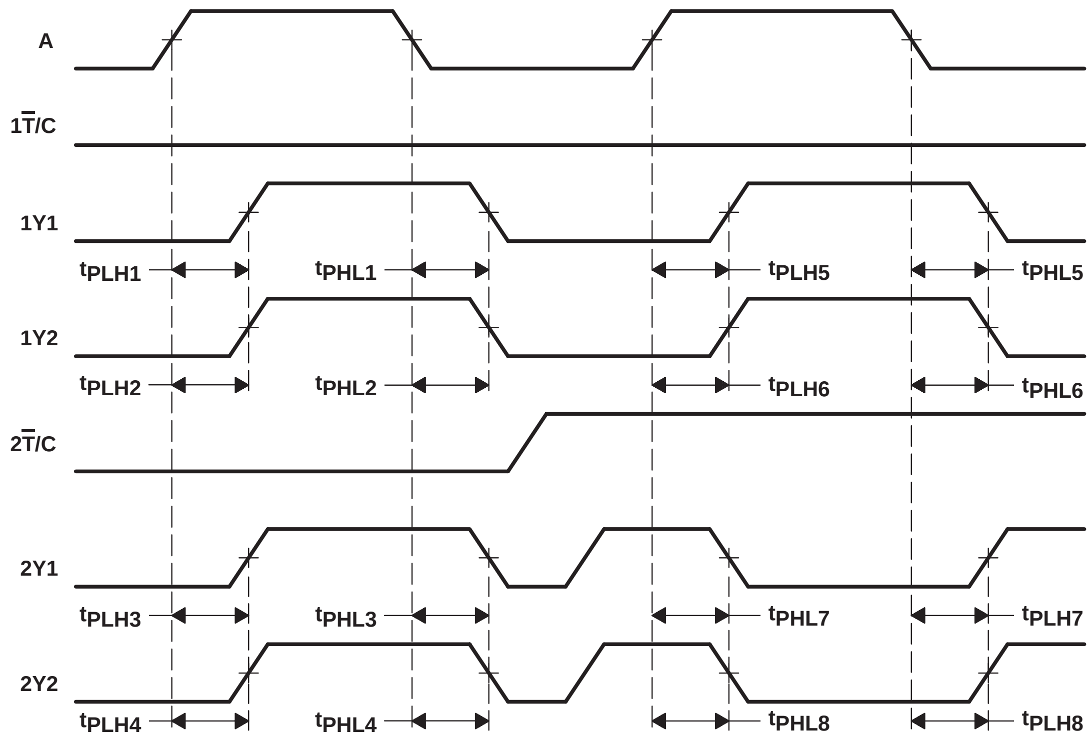


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

C. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, 4, 5, 6 ,7, 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDC328AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC328ADBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
CDC328ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC328ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC328ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC328ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC328ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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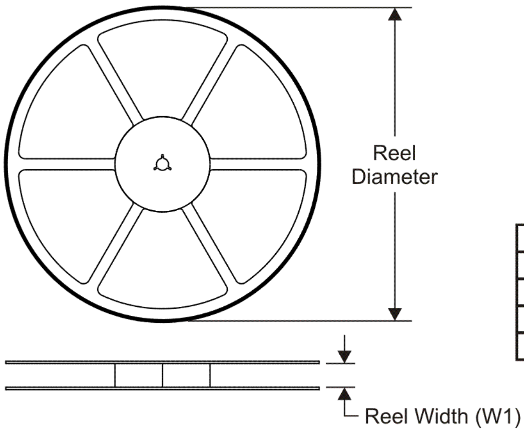
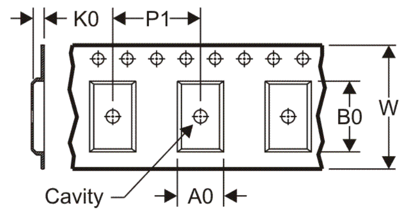
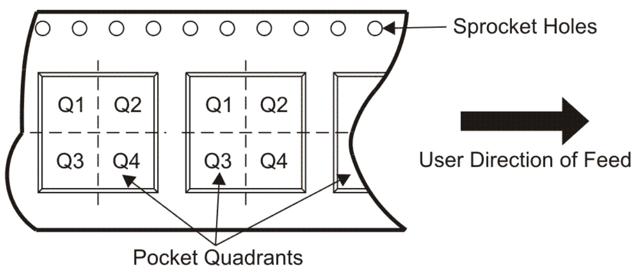
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

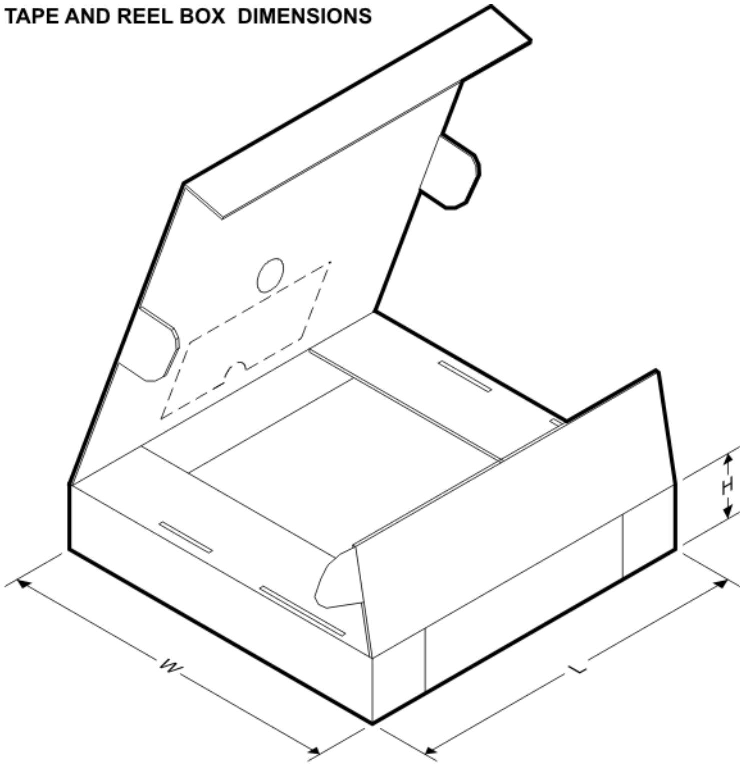
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC328ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
CDC328ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC328ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
CDC328ADR	SOIC	D	16	2500	346.0	346.0	33.0

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